**National College of Computer Studies**

**BIM 3rd Semester 2025 (22nd Batch)**

**Subject: Microprocessor**

**Presentation Topics**

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| **S.N.** | **Name** | **Topic** |
| **1.** | Aarya Tuladhar | **Register Organization** |
| **2.** | Aayush Chaudhary | **Instruction Format** |
| **3.** | Aayush Kumar Singh | **Parallel Processing** |
| **4.** | Ishan Poudel | **Pipelining** |
| **5.** | Lumana Manandhar | **Computer Arithmetic (Addition and Subtraction)** |
| **6.** | Luniva Shilpakar | **Arithmetic Pipeline** |
| **7.** | Minisha Dangol | **Multiplication and Booth’s Algorithm** |
| **8.** | Nikisha Maharjan | **Instruction Pipeline** |
| **9.** | Preshna Thapa | **Division Algorithm Example** |
| **10.** | Raj Gurung | **Arithmetic Logic Shift Unit (ALSU)** |
| **11.** | Regisha Maharjan | **Asynchronous Data Transfer** |
| **12.** | Richina Devi Pradhan | **Modes of Transfer** |
| **13.** | Safalta Joshi | **Priority Interrupt** |
| **14.** | Sailesh Neupane | **Direct Memory Address (DMA)** |
| **15.** | Sakshyam Tamrakar | **Input/Output Processor** |
| **16.** | Sameer Maharjan | **Serial Communication** |
| **17.** | Shaishab Krishna Joshi | **Memory Hierarchy** |
| **18.** | Shikshya Maharjan | **Main Memory** |
| **19.** | Siddhartha Shakya | **Data Transfer and Manipulation** |
| **20.** | Sonika Bohora | **Auxiliary Memory** |
| **21.** | Subina Maharjan | **Associative Memory** |
| **22.** | Sudish Maharjan | **Cache Memory** |
| **23.** | Suhana Shrestha | **Division Algorithm Explanation** |
| **24.** | Sujal Shrestha | **Peripheral Devices** |
| **25.** | Sweta Ranjit | **Addressing Modes** |
| **26.** | Yukesh Maharjan | **Stacks Organization** |